

**METHOD AND APPARATUS FOR ADAPTIVE TIMING  
OPTIMIZATION OF AN INTEGRATED CIRCUIT  
DESIGN**

ABSTRACT OF THE DISCLOSURE

An optimization apparatus and method optimizes a functional block within a netlist of an integrated circuit design. A corresponding delay value is assigned to each of a plurality of pins of the block. Each pin corresponds to a respective signal path through the block. The delay values together form a delay value combination, which is selected from a continuous set of possible combinations in which each combination in the set satisfies a predetermined criteria. A circuit configuration for the block is then generated with a plurality of logic cells that are interconnected in the netlist such that the respective signal paths have delays through the block that are based on the corresponding delay values.

TOP SECRET